We Claim:

1. A method for fabricating a semiconductor component or an interconnect for semiconductor components comprising:

providing a substrate comprising a first side and an opposing second side;

forming a first electrically insulating layer on the first side and a second electrically insulating layer on the second side;

directing a laser beam at the substrate to form a lasered opening through the substrate;

forming a conductive member in the lasered opening;

forming a first external contact on the first electrically insulating layer in electrical communication with the conductive member; and

forming a second external contact on the second electrically insulating layer in electrical communication with the conductive member.

2. The method of claim 1 further comprising providing the substrate with a contact, forming an opening in the contact, and wherein during the directing step the laser beam is directed through the opening without touching the contact.

3. The method of claim 1 further comprising forming non-oxidizing layers on the first external contact and on the second external contact.

4. The method of claim 1 wherein the conductive member comprises enlarged terminal portions for the first external contact and the second external contact.

5. A method for fabricating a semiconductor component or an interconnect for semiconductor components comprising:

providing a substrate comprising a first side, an opposing second side and a contact on the first side;

forming an opening in the contact;

directing a laser beam at the opening and through the substrate to laser drill a via aligned with the opening;

forming a conductive member in the via in electrical communication with the contact;

forming a first external contact on the first side in electrical communication with the conductive member; and

forming a second external contact on the second side in electrical communication with the conductive member.

6. The method of claim 5 wherein the opening surrounds a portion of the substrate and the laser beam pierces the substrate on the portion.

7. The method of claim 5 wherein the contact comprises metal and the laser beam passes through the metal without touching the metal.

8. The method of claim 5 further comprising forming non-oxidizing layers on the first external contact and on the second external contact.

9. The method of claim 5 wherein the first external contact and the second external contact comprise enlarged terminal portions of the conductive members.

10. The method of claim 5 wherein the first external contact and the second external contact comprise concave segments.

11. The method of claim 5 wherein the contact is in electrical communication with integrated circuits on the substrate.

12. The method of claim 5 wherein the substrate comprises a semiconductor die and the contact comprises a bond pad on the die.

13. The method of claim 5 wherein the substrate comprises a semiconductor material and further comprising forming an insulating layer in the via prior to forming the conductive member.

14. A method for fabricating a semiconductor component or an interconnect for semiconductor components comprising:

providing a substrate having a first side and an opposing second side;

forming a mask on the first side having an opening therein;

directing a laser beam at the opening and through the substrate to form a via in the substrate;

depositing a conductive member in the via having a first terminal portion proximate to the first side and a second terminal portion proximate to the second side;

stripping the mask;

forming a first non-oxidizing layer on the first terminal portion; and

forming a second non-oxidizing layer on the second terminal portion,

15. The method of claim 14 further comprising providing the substrate with a contact, etching a second opening in the contact using the opening in the mask, and directing the laser beam at the second opening without touching the contact.

16. The method of claim 14 further comprising forming a first insulating layer on the first side prior to forming the mask and forming the mask on the first insulating layer.

17. The method of claim 14 further comprising forming a second insulating layer on the second side and forming the second external contact on the second insulating layer.

18. The method of claim 14 wherein the substrate comprises a semiconductor material and further comprising electrically insulating the via prior to depositing the conductive member.

19. A method for fabricating a semiconductor component or an interconnect for semiconductor components comprising:

providing a substrate having a first side, an opposing second side and a contact on the first side;

forming an opening in the contact;

directing a laser beam at the opening and through the substrate to form a via aligned with the contact;

forming a conductive member in the via and in the opening having a first terminal portion proximate to the first side, and a second terminal portion proximate to the second side;

forming a first non-oxidizing layer on the first terminal portion; and

forming a second non-oxidizing layer on the second terminal portion.

20. The method of claim 19 further comprising forming a first electrically insulating layer on the first side, forming a second electrically insulating layer on the second side, forming the first non-oxidizing layer on the first electrically insulating layer, and foraying the second non-oxidizing layer on the second electrically insulating layer.

21. The method of claim 19 wherein forming the conductive member comprises electroless deposition and the first terminal portion and the second terminal portion comprise concave segments.

22. The method of claim 19 wherein the substrate comprises a semiconductor die and the contact comprises a bond pad.

23. The method of claim 19 further comprising forming a mask on the substrate, forming the opening using the mask, and stripping the mask following the directing step.

24. The method of claim 19 wherein the substrate comprises a ceramic or a plastic material.

25. The method of claim 19 wherein the substrate comprises a semiconductor material and further comprising electrically insulating the via prior to forming the conductive member.

26. A method for fabricating a semiconductor component comprising:

providing a substrate comprising a first side and an opposing second side;

directing a laser beam at the first side to form a counter bored via in the substrate;

forming a conductive member in the via;

thinning the substrate from the second side to expose the conductive member;

forming a first external contact on the first side in electrical communication with the conductive member; and

forming a second external contact on the second side in electrical communication with the conductive member.

27. The method of claim 26 wherein the thinning step is performed using chemical mechanical planarization.

28. The method of claim 26 wherein the substrate comprises a contact on the first side having an opening therein and the laser beam is directed through the opening without touching the contact.

29. The method of claim 26 wherein the substrate comprises a semiconductor die or wafer.

30. The method of claim 26 wherein the substrate comprises a semiconductor, a ceramic or a plastic.

31. The method of claim 26 further comprising forming a first non-oxidizing metal layer on the first external contact and forming a second non-oxidizing metal layer on the second external contact.

32. A semiconductor component comprising:

a substrate having a first side and an opposing second side;

a conductive member comprising a laser machined via through the substrate, and a conductive material in the via;

a first external contact on the first side comprising a first non-oxidizing layer on the conductive member; and

a second external contact on the second side comprising a second non-oxidizing layer on the conductive member.

33. The component of claim 32 wherein the first external contact and the second external are offset with respect to one another.

34. The component of claim 32 further comprising a substrate contact on the substrate having an opening therein aligned with the via.

35. The component of claim 32 wherein the substrate comprises a semiconductor die comprising a bond pad having an opening therein aligned with the via.

36. The component of claim 32 further comprising a first electrically insulating layer on the first side electrically insulating the first external contact and a second electrically insulating layer on the second side electrically insulating the second external contact.

37. A semiconductor component comprising:

a substrate comprising a first side having a first electrically insulating layer thereon, an opposing second side having a second electrically insulating layer thereon, and a contact with an opening therein on the first side;

a conductive member in electrical communication with the contact, the conductive member comprising a laser machined via through the substrate, and a conductive material at least partially filling the via;

a first external contact on the first electrically insulating layer in electrical communication with the conductive member; and

a second external contact on the second electrically insulating layer in electrical communication with the conductive member.

38. The component of claim 37 wherein the substrate comprises a semiconductor die and the contact comprises a bond pad in electrical communication with integrated circuits on the die.

39. The component of claim 37 wherein the first external contact and the second external contact comprise non-oxidizing layers.

40. The component of claim 37 wherein the first external contact and the second external contact comprise terminal portions of the conductive material.

41. The component of claim 37 wherein the first external contact and the second external contact are offset with respect to one another.

42. An interconnect for a semiconductor component comprising:

a substrate having a first side and an opposing second side;

a laser machined via through the substrate;

a conductive member in the via;

a first external contact on the first side comprising a first non-oxidizing layer on the conductive member; and

a second external contact on the second side comprising a second non-oxidizing layer on the conductive member.

43. The interconnect of claim 42 wherein the first external contact and the second external contact comprise concave terminal portions of the conductive member.

44. An interconnect for a semiconductor component having a bumped contact comprising:

a substrate comprising a first side having a first electrically insulating layer thereon, an opposing second side having a second electrically insulating layer thereon, and a contact with an opening therein on the first side;

a laser machined via through the substrate;

a conductive member in the via in electrical communication with the contact;

a first external contact on the first electrically insulating layer in electrical communication with the conductive member and configured to electrically engage the bumped contact; and

a second external contact on the second electrically insulating layer in electrical communication with the conductive member and configured to provide an electrical path to test circuitry.

45. The interconnect of claim 44 wherein the first external contact and the second external contact comprise non-oxidizing layers.

46. The interconnect of claim 44 wherein the first external contact and the second external contact comprise terminal portions of the conductive material.

47. The interconnect of claim 44 wherein the first external contact and the second external are offset with respect to another.

48. An electronic assembly comprising:

an interconnect comprising:

a substrate having a first side and an opposing second side;

a laser machined via through the substrate;

a conductive member in the via;

a first external contact on the first side comprising a first non-oxidizing layer on the conductive member; and

a second external contact on the second side comprising a second non-oxidizing layer on the conductive member; and

a first semiconductor component having a bumped contact bonded to the first external contact.

49. The electronic assembly of claim 48 further comprising a second semiconductor component having a bumped contact bonded to the second external contact.

50. A test system for a semiconductor component having a bumped contact comprising:

a testing circuitry configured to apply test signals to the component;

an interconnect comprising:

a substrate comprising a first side having a first electrically insulating layer thereon, and an opposing second side having a second electrically insulating layer thereon;

a laser machined via through the substrate;

a conductive member in the via in electrical communication with the contact;

a first external contact on the first electrically insulating layer comprising a concave terminal portion of the conductive member configured to electrically engage the bumped contact; and

a second external contact on the second electrically insulating layer in electrical communication with the conductive member and configured to provide an electrical path to the test circuitry.

51. The test system of claim 50 wherein the component comprises a semiconductor die or a semiconductor package.

52. The test system of claim 51 further comprising a force applying mechanism configured to bias the die or the package together.

53. The test system of claim 50 wherein the component comprises a semiconductor wafer.

54. The test system of claim 52 further comprising a spring loaded electrical connector in electrical communication with the testing circuitry and in physical contact with the second external contact.